

b) for each combination of said slots, identifying the edges intersected by the connection graph or graphs for that particular combination of slots, wherein a plurality of the identified edges are diagonal; and

c) storing the plurality of identified edges for each combination of slots in a storage structure.

68. (Amended) The method of claim 67, wherein a plurality of the edges are horizontal, and a plurality are vertical.

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#### REMARKS

Reconsideration of the patent application in view of the preceding amendments and the following remarks is respectfully requested.

##### **I. Objection To The Drawings**

In the office action dated November 7, 2002, the Draftsperson objected to the drawings. Specifically, the Draftsperson stated that the top margin for **Figures 3, 25, 27, 29, 30A, 34, 37, 39, 40, 43 and 48B** were not acceptable. Applicants have resubmitted the subject figures with corrected margins and respectfully request approval of them.

## **II. Objection To The Specification**

In the office action dated November 7, 2002, the Examiner objected to the title of the application due to a hyphen between the words “Integrated” and “Circuit.” With this Response, Applicants have replaced the title such that the hyphen no longer appears.

## **III. Objection To The Claims**

In the office action dated November 7, 2002 the Examiner objected to claims 28, 43, 58, and 67 due to two types of informalities: claims 58 and 57 contained a hyphen between the words “IC” and “layout”; and, claims 28, 43, 58, and 67 referred to “**the** topology of interconnect lines” rather than “**a** topology of interconnect lines.” Applicants have corrected these informalities through amendment to the subject claims.

## **IV. Rejection of the Claims Under 35 U.S.C. § 112, second paragraph**

In the office action dated November 7, 2002 the Examiner rejected claims under 35 U.S.C. § 112, second paragraph. Specifically, the Examiner rejected claims 28, 29, 43, 44, 58, 59, 67 and 68 due to the use of the word “some” in referencing the use of edges or line paths. Claims 28, 31, 43, 58, and 67 were further rejected as being unclear with respect to the nature of particular elements.

Applicants have amended claims 28, 29, 43, 44, 58, 59, 67, and 68 to recite “a plurality” rather than “some.” These amendments are fully supported by the specification as originally filed, for example at **Figures 13-15** and at **Figures 24-29**. Applicants respectfully submit that the amendments obviate the Examiner’s rejections.

Applicants have further amended claims 28, 31, 43, 58, and 67 as follows: claim 28 now recites “d) identifying the edges, from a plurality of edges, . . .”; claim 31 now recites “the plurality of edges . . .”; claim 43 now recites “d) identifying the plurality of line paths . . .”; claim 58 now recites “c) storing the plurality of identified line paths . . .”; and, claim 67 now recites “c) storing the plurality of identified edges . . .” Applicants respectfully submit that the amended claims are definite under 35 U.S.C. § 112.

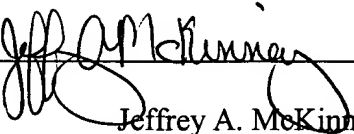
### CONCLUSION

In view of the foregoing, it is submitted that the claims are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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22                    29.     (Amended)     The method of claim 28, wherein [some] a plurality  
23 of said edges are horizontal and [some] a plurality are vertical.

24

25                    31.     (Amended)     The method of claim 30, wherein the plurality of  
26 edges are defined based on a wiring model for the IC layout and on a partitioning  
27 structure defined by the partitioning lines.

28

29                    43.     (Amended)     A method of placing circuit modules in a region of  
30 an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements,  
31 wherein a plurality of nets represent interconnections between said circuit elements, each  
32 net defined to include a set of circuit elements, the method comprising:

33                    a)       partitioning the IC region into several sub-regions, wherein a  
34 plurality of line paths exist between said sub-regions, wherein [some] a plurality of said  
35 line paths are diagonal;

36                    b)       selecting a net;

37                    c)       identifying the set of sub-regions containing the circuit elements of  
38 the selected net;

39                    d)       identifying the plurality of line paths used by at least one  
40 connection graph that represents [the] a topology of one or more interconnect lines  
41 necessary for connecting the identified set of sub-regions, wherein at least one of the  
42 identified line paths is diagonal; and

43 e) computing a placement cost by using the identified line paths.

44

45 44. (Amended) The method of claim 43, wherein [some] a plurality  
46 of said line paths are horizontal and [some] a plurality are vertical.

47

48 58. (Amended) For an electronic-design-automation placer that uses  
49 a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit  
50 ("IC") layout region into a plurality of sub-regions corresponding to said slots, wherein a  
51 plurality of line paths exist between said slots, a method of pre-computing costs of  
52 placing circuit modules in an IC layout region, the method comprising:

53 a) for each combination of said slots, identifying at least one  
54 connection graph that represents [the] a topology of interconnect lines necessary for  
55 connecting the combination of said slots;

56 b) for each combination of said slots, identifying the line paths used  
57 by the connection graph or graphs for that particular combination of slots, wherein [some]  
58 a plurality of the identified line paths are diagonal; and

59 c) storing the plurality of identified line paths for each combination of  
60 slots in a storage structure.

61

62 59. (Amended) The method of claim 58, wherein [some] a plurality  
63 of the line paths are horizontal, and [some] a plurality are vertical.

64

65                    67.     (Amended)     For an electronic-design-automation placer that uses  
66     a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit  
67     (“IC”) layout region into a plurality of sub-regions corresponding to said slots, wherein a  
68     plurality of edges exist between said slots, a method of pre-computing costs of placing  
69     circuit modules in an IC layout region, the method comprising:

70                    a)        for each combination of said slots, identifying at least one  
71     connection graph that represents [the] a topology of interconnect lines necessary for  
72     connecting the combination of said slots;

73                    b)        for each combination of said slots, identifying the edges intersected  
74     by the connection graph or graphs for that particular combination of slots, wherein [some]  
75     a plurality of the identified edges are diagonal; and

76                    c)        storing the plurality of identified edges for each combination of  
77     slots in a storage structure.

78  
79                    68.     (Amended)     The method of claim 67, wherein [some] a plurality  
80     of the edges are horizontal, and [some] a plurality are vertical.